SONY

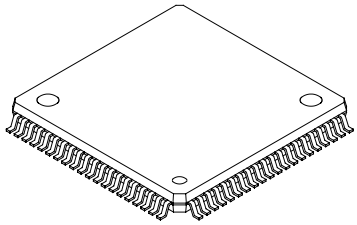
CXB1590Q

SDH 8 bit 622 Mbps Transceiver

Description

The CXB1590Q is a transceiver IC with built-in PLL for ATM network. For a receiver 622 Mbps serial data is received and output it as the 8-bit parallel data; for a transmitter 622 Mbps 8-bit parallel data is output as the serial data.

80 pin QFP (Plastic)



Features

- Transmitter and receiver in a single chip
- TTL/ECL compatible
- Single +3.3 V power supply
- PLL for clock generation and clock / data recovery
- 8:1 Parallel/Serial Converter, 1:8 Serial/Parallel Converter, Frame (A1/A1/A1/A2/A2/A2, A1 : 11110110, A2 : 00101000) detector
- Selectable 4 modes input/output REFCLK (19.44, 25.92, 51.84, 77.76 MHz)
- Adjustable timing between input parallel data and transmitting parallel clock
- Lock detector for a receiver PLL
- Selectable ECL-output 4 signals (retimed data, transmitted bit rate clock, recovered bit rate clock, received serial data through) in a test mode
- Selectable operation clock of transmitter site recovered bit rate clock in a test mode
- Local loop back circuit (parallel data to parallel data)
- Low power consumption (1.0 W typical)
- 80-pin plastic QFP package (body size : 14 mm × 14 mm)

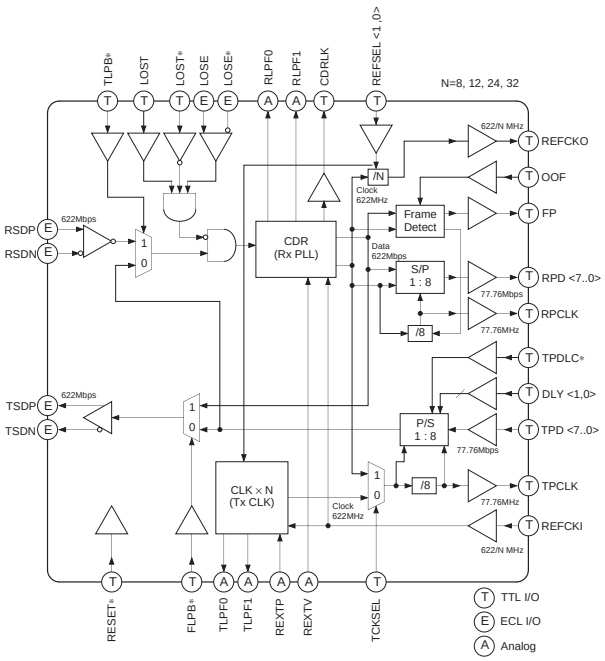


Fig. 1 Block Diagram

E97905A83-TE

Table 1 Absolute Maximum Ratings (VEEE, VEET, VEEG, VEEP=GND)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	VCC	–0.3		4.0	V	
TTL DC input voltage	VI_T	–0.5		5.5	V	
ECL DC input voltage	VI_E	VCC–2.0		VCC	V	
ECL peak-to-peak differential input voltage swing	VIS_E	–4.0		4.0	V	
TTL output current (High)	IOH_T	–20		0	mA	
TTL output current (Low)	IOL_T	0		20	mA	
ECL output current	IO_E	–30		0	mA	
Ambient temperature	Ta	–55		70	°C	Under bias
Storage temperature	Tstg	–65		150	°C	

Table 2 Recommended Operating Conditions (on PCB with 2 planes, no air flow)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Power supply voltage	VCC	3.135	3.3	3.465	V	
Ambient temperature	Ta	0		70	°C	

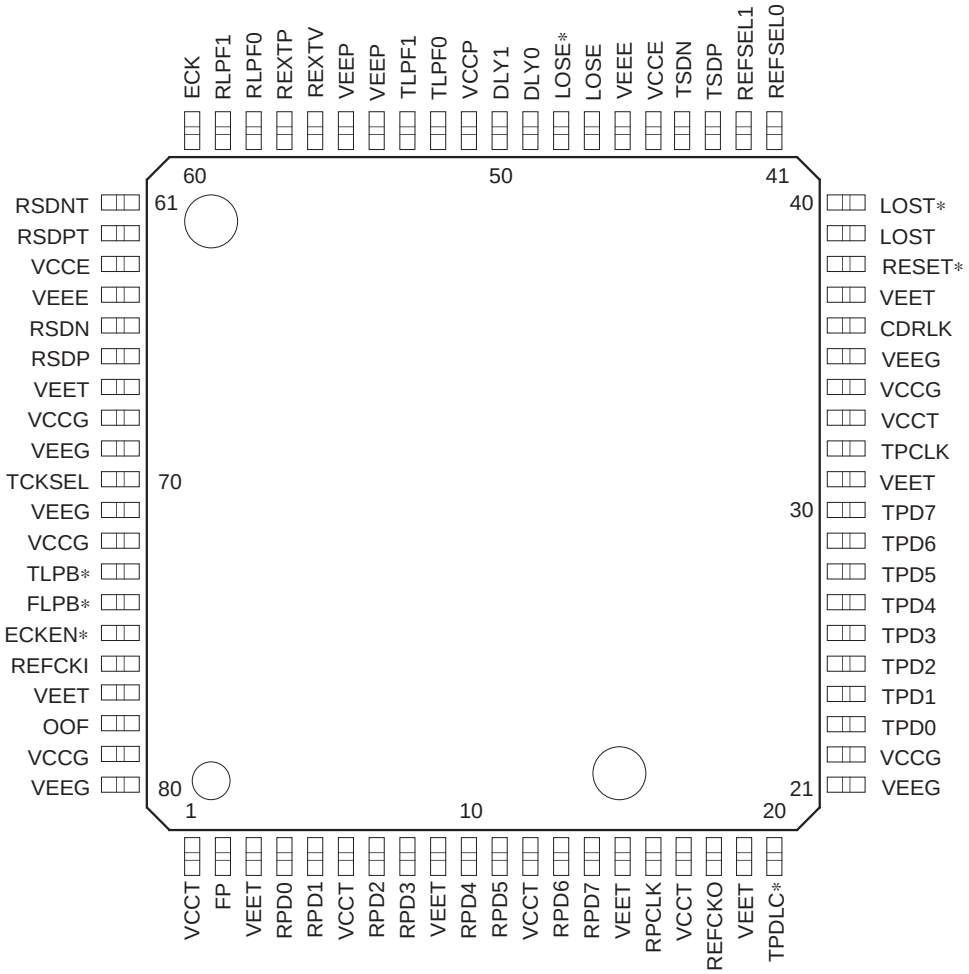


Fig. 2 Pin Configuration (Top View)

Table 3 DC Characteristics (Under the recommended conditions. See Table 2.)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Input HIGH voltage (TTL)	VIH_T	2.0		5.5	V	
Input LOW voltage (TTL)	VIL_T	0.0		0.8	V	
Input HIGH current (TTL)	IIH_T			20	µA	Vin=VCC
Input LOW current (TTL)	IIL_T	–400			µA	Vin=0
Output HIGH voltage (TTL)	VOH_T	2.2			V	IOH=–0.4mA
Output LOW voltage (TTL)	VOL_T			0.5	V	IOL=2mA
Input HIGH voltage (ECL)	VIH_E	VCC–1.17		VCC–0.88	V	
Input LOW voltage (ECL)	VIL_E	VCC–1.81		VCC–1.48	V	
Peak-to-peak differential input voltage swing (ECL)	VIS_E 1)	100		2000	mV	AC coupled
Output HIGH voltage (ECL)	VOH_E	VCC–1.30		VCC–0.81	V	50 Ω to VCC–2 V
Output LOW voltage (ECL)	VOL_E	VCC–1.90		VCC–1.55	V	50 Ω to VCC–2 V
Peak-to-peak differential output voltage swing (ECL)	VOS_E 2)	1200		2000	mV	
Supply current	ICC	224	296	412	mA	Outputs open
Power dissipation	Pd	694	977	1442	mW	Outputs open

Note :

1) Peak-to-peak differential input voltage swing (ECL)

2) Peak-to-peak differential output voltage swing (ECL)

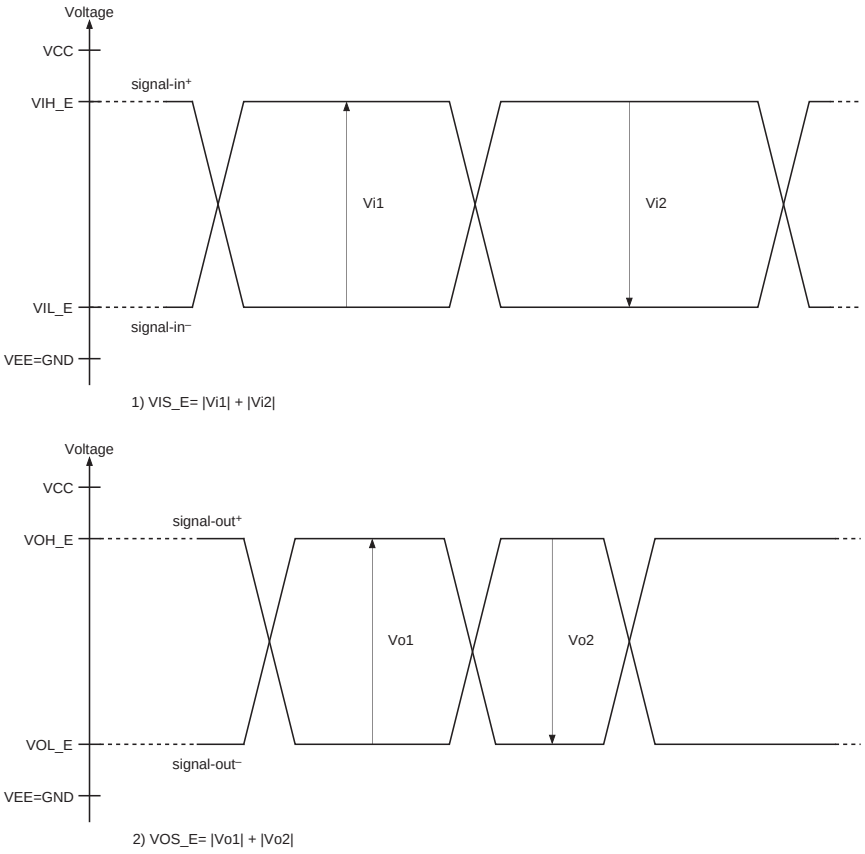


Fig. 3 ECL peak-to-peak differential input/output voltage swing

Table 4 AC Characteristics (Under the recommended conditions. See Table 2.)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Operating Frequency	Fop	600	622	650	Mbps	
Input TTL rise time of TX	Tir_TX	0.7		4.8	ns	0.8 V to 2.0 V
Input TTL fall time of TX	Tif_TX	0.7		4.8	ns	2.0 V to 0.8 V
Input TTL rise time of REFCKI	Tir_REF	0.7		2.4	ns	0.8 V to 2.0 V
Input TTL fall time of REFCKI	Tif_REF	0.7		2.4	ns	2.0 V to 0.8 V
Output TTL rise time	Tor_T			3.5	ns	0.8 V to 2.0 V, CL=10 pF
Output TTL fall time	Tof_T			3.5	ns	2.0 V to 0.8 V, CL=10 pF
Output ECL rise time	Tor_E			400	ps	20 % to 80 %, CL=2 pF
Output ECL fall time	Tof_E			400	ps	20 % to 80 %, CL=2 pF
Duty Cycle of REFCKI	DC_RCI	33		67	%	
RPD setup time to RPCLK rise	Ts_RPD	3.0			ns	CL=10 pF
RPD hold time to RPCLK rise	Th_RPD	5.5			ns	CL=10 pF
FP setup time to RPCLK rise	Ts_FP	3.5			ns	CL=10 pF
FP hold time to RPCLK rise	Th_FP	5.0			ns	CL=10 pF
TPD setup time to TPCLK rise	Ts_TPD	3.6			ns	timing mode : DLY0
		5.4			ns	timing mode : DLY1
		8.3			ns	timing mode : DLY3
		11.6			ns	timing mode : DLY5
		14.5			ns	timing mode : DLY7
TPD hold time to TPCLK rise	Th_TPD	0.0			ns	timing mode : DLY0
		–1.8			ns	timing mode : DLY1
		–4.8			ns	timing mode : DLY3
		–8.0			ns	timing mode : DLY5
		–10.9			ns	timing mode : DLY7
Duty Cycle of REFCKO	DC_RCO	40		60	%	in frequency lock
Duty Cycle of RPCLK	DC_RPC	40		60	%	in frequency lock
TSDP/TSDN Deterministic jitter (p-p)	TxDJ			55	deg	Serial data output
TSDP/TSDN Random jitter (rms)	TxRJ			5.5	deg	Serial data output
Clock generator PLL band width	TxBW	600		5300	kHz	OC-12 template
		500		4500	kHz	STM-4 template
Recovered clock Random jitter (rms)	RxRj			6.5	deg	R4=R5=620 Ω
				6.0	deg	R4=R5=1 kohm
CDR PLL band width	RxBW			700	kHz	OC-12 Template, R4=R5=620 Ω
				700	kHz	STM-4 template, R4=R5=620 Ω
				1100	kHz	OC-12 template, R4=R5=1 kΩ
				1100	kHz	STM-4 template, R4=R5=1 kΩ
Jitter Tolerance	JT			0.7	UI	Serial data input

Table 5 PLL AC Characteristics (Under the recommended conditions. See Table 2.)

Description	Symbol	Min.	Typ.	Max.	Unit	Conditions
Frequency Acquisition Time of TX PLL	Tfa			1000	µs	Loop Damping Capacitor=0.022 µF
Bit Synchronization Time of RX PLL	Tbs			6500	bit	

Table 6 Pin Description

Pin No.	Pin Name	Type	Description	Equivalent circuit
66 65	RSDP RSDN	I_ECL	Received serial data (RSDP/RSDN) are the differential input of 622 Mbps Rx bit stream.	(c)
39	LOST	I_TTL	Loss of signal (LOST/LOST∗, LOSE/LOSE∗) indicate that RSDP/RSDN dosen't exist in order to prevent the PLL from runaway. RSDP/RSDN are masked and RxPLL goes training mode when LOST=H and LOST∗=L and LOSE/LOSE∗=H/L.	(a)
40	LOST∗	I_TTL		(a)
47 48	LOSE LOSE*	I_ECL		(c)
73	TLPB∗	I_TTL	Terminal loop back (TLPB∗) switch the RxPLL input to the loop backed signal form P/S converter when it's Low.	(a)
36	CDRLK	O_TTL	Clock data recovery in lock (CDRLK) indicate that RxPLL is lock to Rx bit stream. It's active-high.	(b)
18	REFCKO	O_TTL	Reference clock output (REFCKO) is 622/N MHz clock made from the recovered clock by RxPLL.	(b)
16	RPCLK	O_TTL	Received parallel clock (RPCLK) is 77.76 MHz clock made from the recovered clock by RxPLL. It provides timing of RPD <7..0> and FP.	(b)
4, 5, 7, 8, 10, 11, 13, 14	RPD <0..7>	O_TTL	Received parallel data (RPD <7..0>) are the bus of 77.76 Mbps Rx byte stream. RPD7 is the first bit received, RPD0 is the last. They should be latched on the rising edge of RPCLK.	(b)
2	FP	O_TTL	Frame position (FP) indicate the 3rd A2 byte in ATM frame header. It is active-high signal.	(b)
78	OOF	I_TTL	Out of frame (OOF) enable the frame detector to find A1/A1/A1/A2/A2/A2 stream in RSDP/RSDN, output the flag to FP and establish the boundary when it's High. The frame detector dosen't output flag or re-establish the byte boundary when it's low.	(a)
76	REFCKI	I_TTL	Reference clock input (REFCKI) is the 622/N MHz clock for transmitting clock source. TxPLL multiply it by N to generate the transmitting clock. It's also used for RxPLL training when loss of signal.	(a)
32	TPCLK	O_TTL	Transmitting parallel clock (TPCLK) is 77.76 MHz clock made from the transmitting clock by the divider. It provides timing of TPD <7..0>.	(b)
23-30	TPD <0..7>	I_TTL	Transmitting parallel data (TPD <7..0>) are the bus of 77.76 Mbps Tx byte stream. TPD7 is the first bit transmitting, TPD0 is the last. They are latched on the rising edge of TPCLK when TPDLC∗=High. The latch timing is adjustable when TPDLC∗=Low by DLY <1, 0>.	(a)

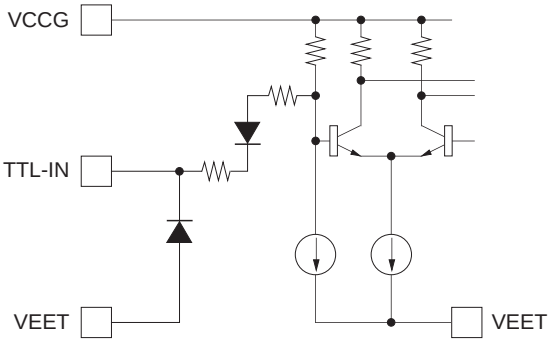
Pin No.	Pin Name	Type	Description	Equivalent circuit
20	TPDLC∗	I_TTL	Transmitting parallel data latch control (TPDLC∗) enable the timing adjust between TPCLK and TPD <7..0> by DLY <1,0>. It's active-low.	(a)
49	DLY0	I_TTL	DLY <1, 0> act as timing adjuster between TPCLK and TPD <7..0> when TPDLC∗=Low. They should be open or High when TPDLC∗=High, other setting is for testing in fabrication.	(a)
50	DLY1	I_TTL		(a)
43 44	TSDP TSDN	O_ECL	Transmitting serial data (TSDP/TSDN) are the differential output of 622 Mbps Tx bit stream.	(e)
74	FLPB∗	I_TTL	Facility loop back (FLPB∗) enable the direct loop back from RSDP/RSDN to TSDP/TSDN when it's Low.	(a)
41	REFSEL0	I_TTL	REFSEL <1, 0> control N to select the Reference clock frequency. N=8, 12, 24, 32. (REFCKI=77.76, 51.84, 25.92, 19.44 MHz.)	(a)
42	REFSEL1	I_TTL		(a)
62 61	RSDPT RSDNT	EX	Received serial data through (RSDPT/RSDNT) are connected to RSDP/RSDN through the chip for ECL signal termination.	—
58 59	RLPF0 RLPF1	EX	Rx loop filter (RLPF0/RLPF1). They should be tied via external LPF devices (-R-C-R).	(f)
52 53	TLPF0 TLPF1	EX	Tx loop filter (TLPF0/TLPF1). They should be tied via external LPF devices (-R-C-R).	(f)
56	REXTV	EX	External resistor for VCO (REXTV). It should be tied to VEEP via external resistor to setting the center frequency of VCO in both RxPLL and TxPLL.	(g)
57	REXTP	EX	External resistor for charge pump (REXTP). It should be tied to VEEP va external resistor to setting the charge-pump current of RxPLL.	(h)
38	RESET∗	I_TTL	Reset (RESET∗) is the active-low reset. It's for testing in the fabrication. Leave it open in normal operation.	(a)
70	TCKSEL	I_TTL	Transmitting clock act as the recovered clock when it's Low. Leave it open in normal operation.	(a)
60	ECK	I_ECL	External clock (ECK) act as the transmitting and recovered clock input when ECKEN∗=Low. It's for testing in the fabrication. Leave it open in normal operation.	(d)
75	ECKEN∗	I_TTL	External clock enable (ECKEN∗) enable the ECK when it's Low. It's for testing in the fabrication. Leave it open in normal operation	(a)

Pin No.	Pin Name	Type	Description	Equivalent circuit
45, 63	VCCE	PS	Power supply for ECL output : Normally 3.3 V	—
1, 6, 12, 17, 33	VCCT	PS	Power supply for TTL output : Normally 3.3 V	—
22, 34, 68, 72, 79	VCCG	PS	Power supply for internal logic gates : Normally 3.3 V	—
51	VCCP	PS	Power supply for PLL : Normally 3.3 V	—
46, 64	VEEE	PS	Ground for ECL output : Normally 0 V	—
3, 9, 15, 19, 31, 37, 67, 77	VEET	PS	Ground for TTL output : Normally 0 V	—
21, 35, 69, 71, 80	VEEG	PS	Ground for internal logic gates : Normally 0 V	—
54, 55	VEEP	PS	Ground for PLL : Normally 0 V	—

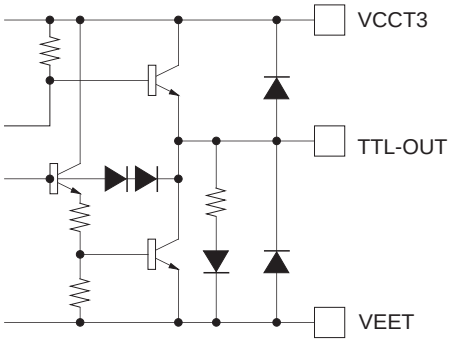
Table 7 Pin Type Definition

Type	Definition
PS	Power supply or ground
I_TTL	Input TTL
O_TTL	Output TTL
I_ECL	Input ECL
O_ECL	Output ECL
EX	External circuit node

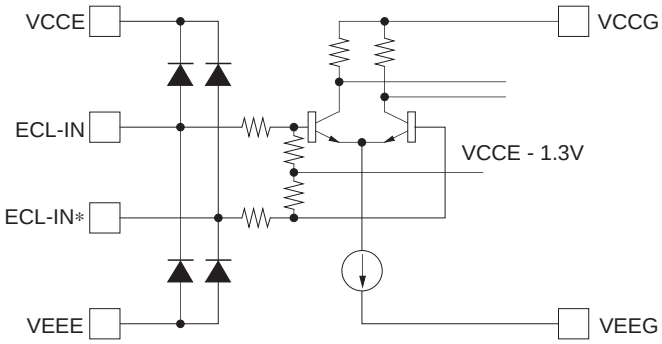
Equivalent Circuit



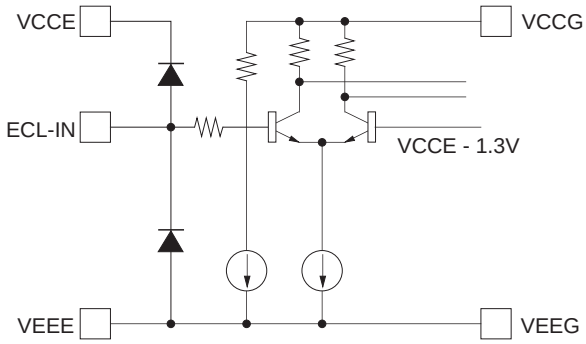
(a) TTL input equivalent circuit



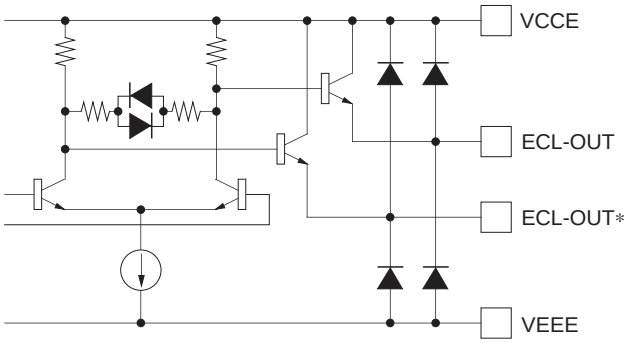
(b) TTL output equivalent circuit



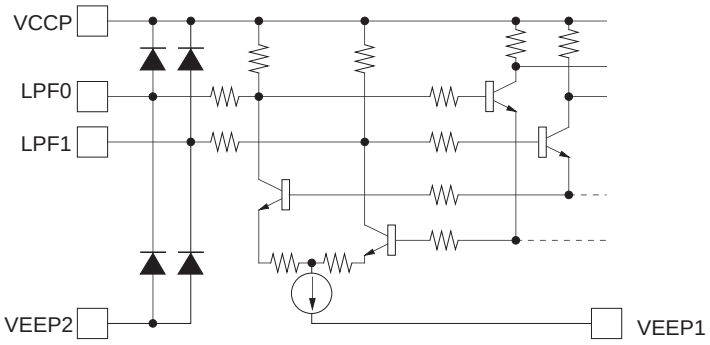
(c) ECL input equivalent circuit (differential)



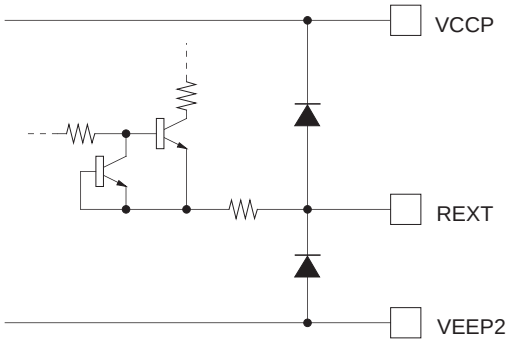
(d) ECL input equivalent circuit (single)



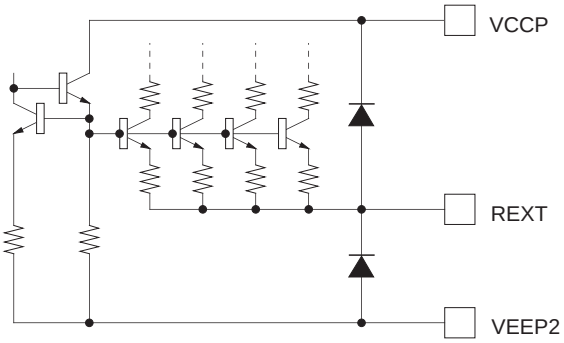
(e) ECL output equivalent circuit



(f) LPF0/LPF1-pin equivalent circuit



(g) REXTV-pin equivalent circuit



(h) REXTP-pin equivalent circuit

Fig. 4 Equivalent CIrcuit

Selection Table

Table 8 Input Data to RxPLL Selection Table

TLPB*	TPDLC*	DLY0	DLY1	Input data to RxPLL
1	X	X	X	RSDP/RSDN
0	X	1	1	Serial-data from P/S-conv.
0	0	X	X	

Table 9 Monitor Output (TSDP/TSDN) Selection Table

FLPB*	TPDLC*	DLY0	DLY1	TSDP/TSDN
0	X	X	X	Rx retimed data
1	1	0	0	Recovered bit rate clock
1	1	0	1	Transmitted bit rate clock
1	0	X	X	Serialized data
1	X	1	1	
1	1	1	0	RSDP/RSDN

Table 10 Reference Clock Frequency Selection Table

REFSEL0	REFSEL1	REFCKI-Frequency
0	0	77.76 MHz
0	1	51.84 MHz
1	0	19.44 MHz
1	1	25.92 MHz

I/O Timing

1. Transmitter

Transmitting parallel clock (TPCLK) is 77.76 MHz clock made from transmitting clock by the divider. It provides timing of TPD<7..0>.

Transmitting parallel data (TPD<7..0>) are the bus of 77.76 Mbps Tx byte stream. TPD is converted into output-serial-data by P/S converter.

Timing between TPCLK and TPD<7..0> is able to adjust by another inputs (TPDLC∗, DLY0, DLY1). This timing has 5 kinds ; DLY0, DLY1, DLY3, DLY5, DLY7.

Timing of TPD for TPCLK (set up, hold time) is shown in Fig. 5 and Table 11.

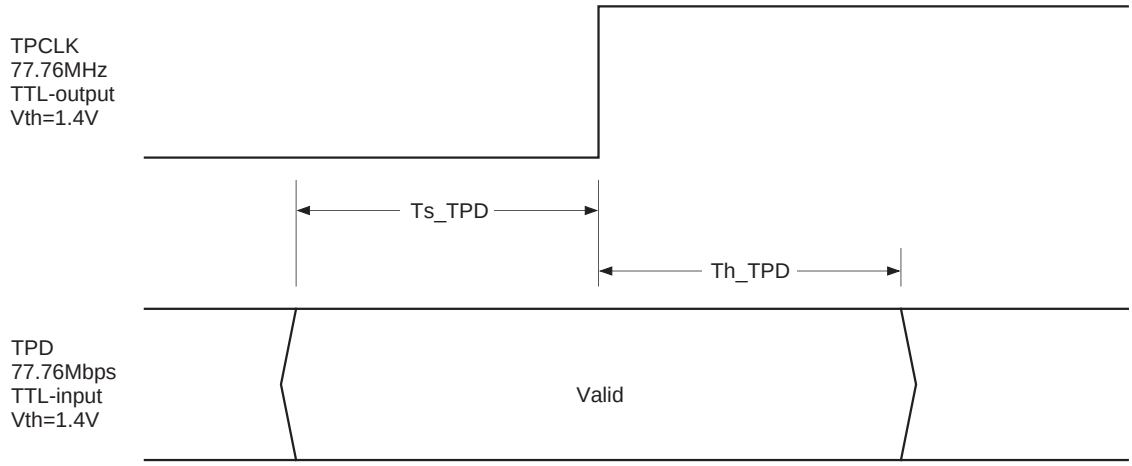


FIg. 5 Transmitter Section Timing

Table 11 Timing Mode Selection Table

TPDLC∗	DLY0	DLY1	timing	Ts_TPD (nsec)	Th_TPD (nsec)
1	X	X	DLY0	3.6	0.0
0	0	0	DLY1	5.4	–1.8
0	1	0	DLY3	8.3	–4.8
0	0	1	DLY5	11.6	–8.0
0	1	1	DLY7	14.5	–10.9

2. Receiver

Received parallel clock (RPCLK) is 77.76 MHz clock extracted from the recovered data by RxPLL. It provides timing of RPD<7..0> and FP.

Received parallel data (RPD<7..0>) are the bus of 77.76 Mbps Rx byte stream. Input-serial-data is converted into RPD by S/P converter with RPCLK.

When OOF is set “High”, frame position (FP) indicate the 3rd A2 byte in ATM frame header. FP is active high signal which is detected by frame-detector, and width of active high signal is 1 byte.

Timing of RPD and FP for RPCLK are shown in Fig. 5. And bounds of “OOF=1” for enable FP detection is shown in Fig. 6.

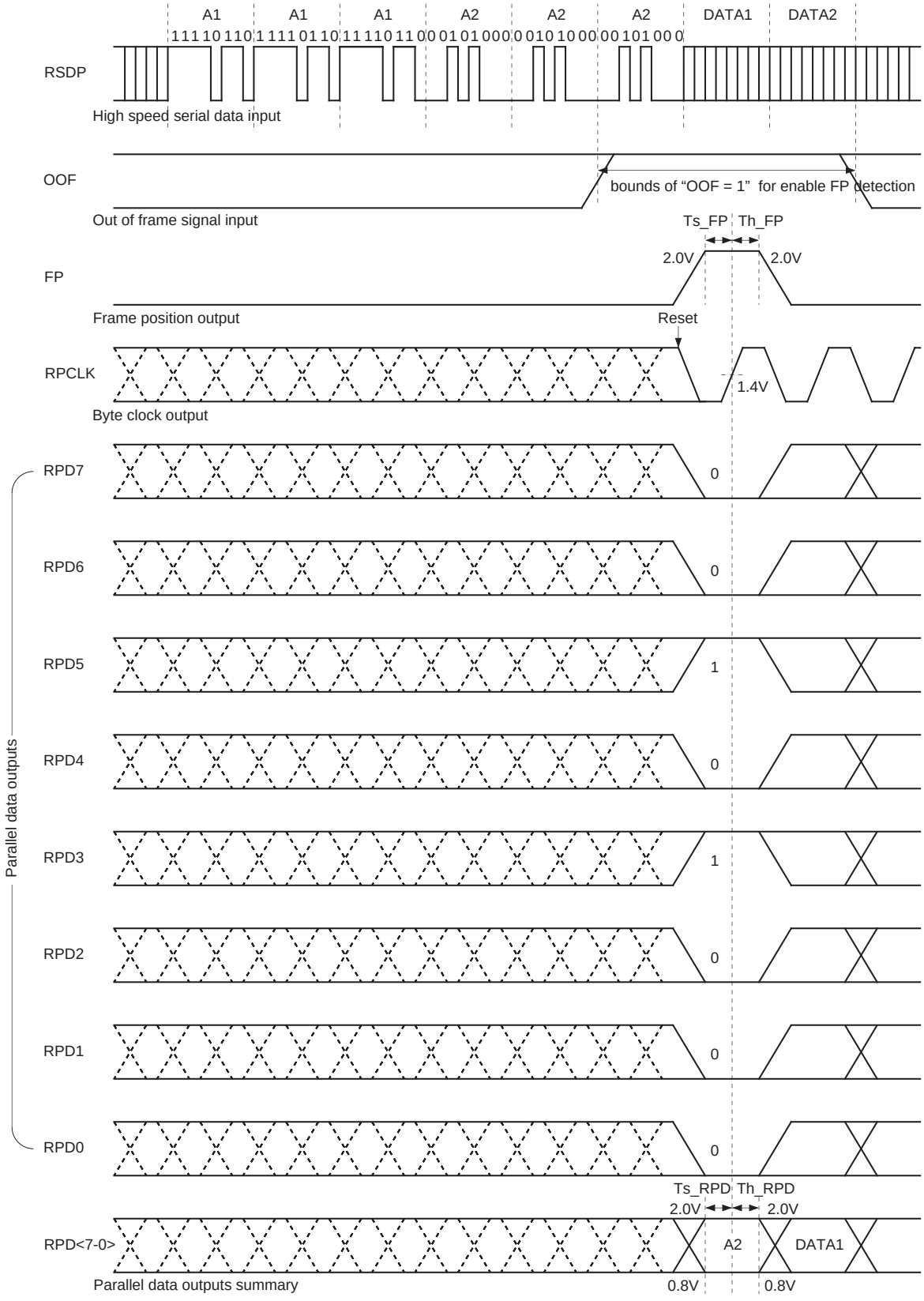


Fig. 6 Receiver Section Timing

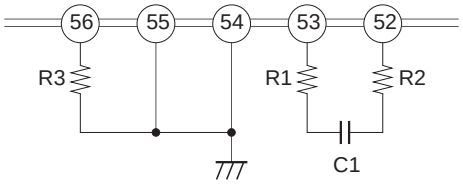
Notes on Operation

1. External Components PLLs

CXB1590Q is the transceiver. It has the clock synthesizer for the transmitter and the clock recovery circuit for the receiver.

(1) Clock Synthesizer

CXB1590Q has the internal clock synthesizer based on PLL, which locks to REFCKI and generates bit rate clock frequency. It needs external loop filter and a resistor which determines the free-run frequency of VCO. Typical values of external components are indicated below. To minimize temperature dependency in VCO frequency, C1 should be a capacitor with less temperature coefficient.

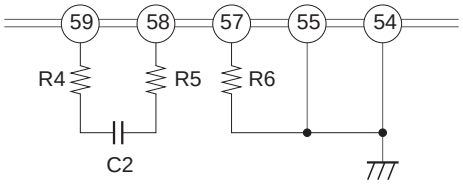


f_{REFCLK} (MHz)	19.44	25.92	51.84	77.76
R1 (Ω)	2.7 k	2.0 k	1.0 k	680
R2 (Ω)	2.7 k	2.0 k	1.0 k	680
R3 (Ω)	1.5 k			
C1 (F)	22 n			

Fig. 7 External Loop Filter and Resistor for Tx-PLL

(2) Clock Recovery Circuit

CXB1590Q has internal clock recovery circuit based on the PLL which locks to incoming data stream. It needs external loop filter and the resistor which determines the current of the charge pump. Typical values of external components are indicated below. There are two-sets recommended values ; (1) the one is to minimization jitter generation, (2) the another is to be satisfied the template (STM-4, OC-12) in jitter transfer measurement. To minimize temperature dependency in VCO frequency, C2 should be a capacitor with less temperature coefficient.

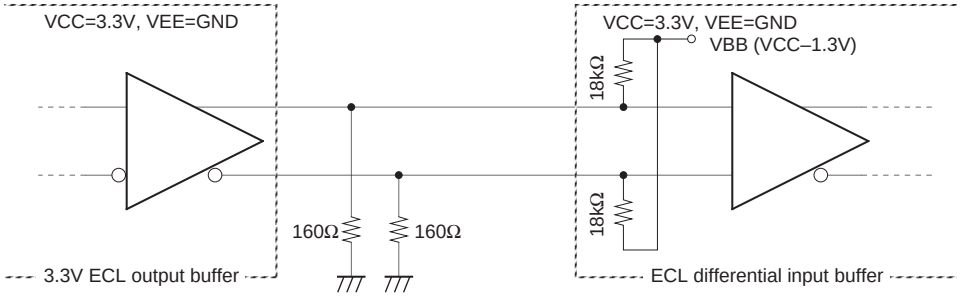


	(1)	(2)
R4 (Ω)	1.0 k	620
R5 (Ω)	1.0 k	620
R6 (Ω)	680	
C2 (F)	68n	

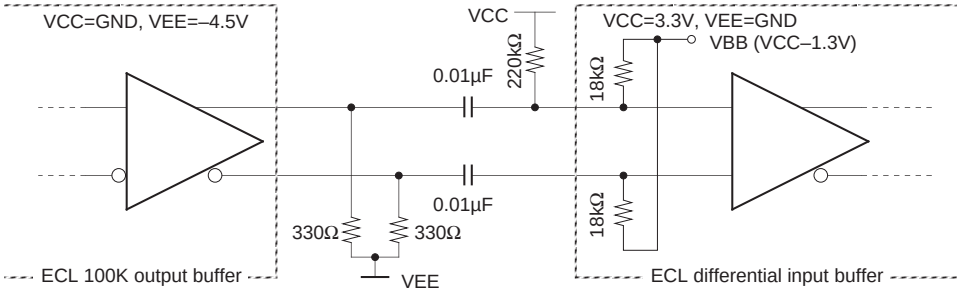
Fig. 8 External Loop Filter and Resistor for Rx-PLL

2. High speed ECL compatible differential input

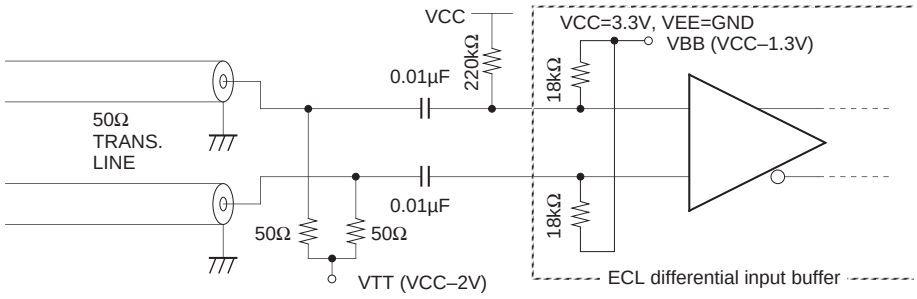
The high speed ECL compatible differential inputs in CXB1590Q is biased to VBB (VCC–1.3 V) with 18 kΩ. High speed input applications are shown in Fig. 9.



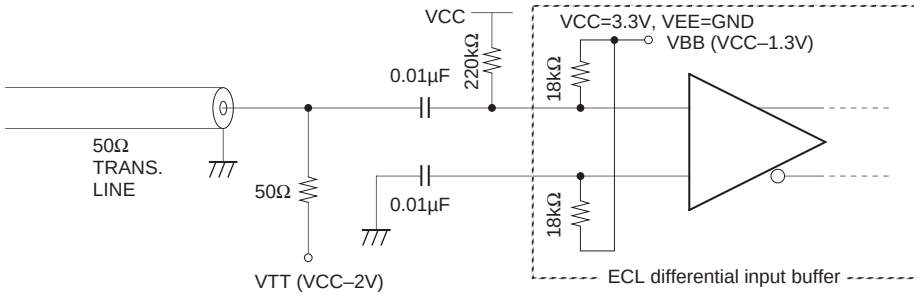
(a) ECL differential signal from 3.3 V ECL output buffer



(b) ECL differential signal from ECL 100 K output buffer



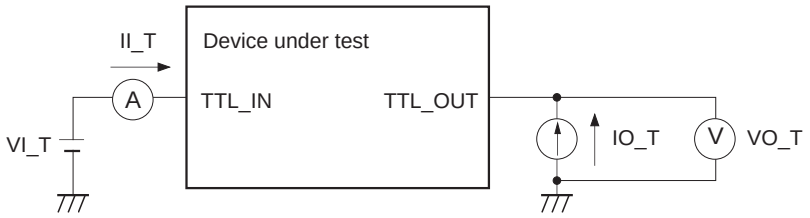
(c) ECL differential signal form 50 Ω transmission line



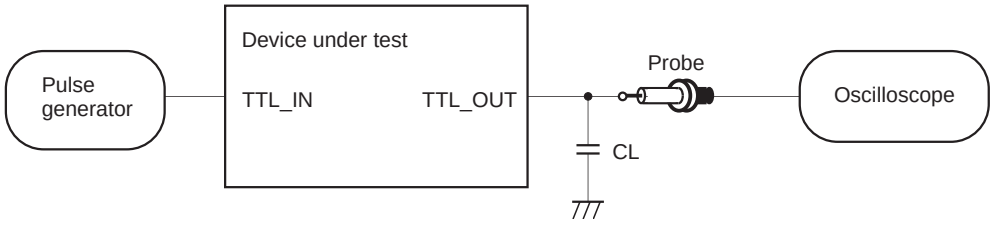
(d) ECL single signal from 50 Ω transmission line

Fig. 9 High Speed Input Application

3. Electrical Characteristics Measurement Circuit

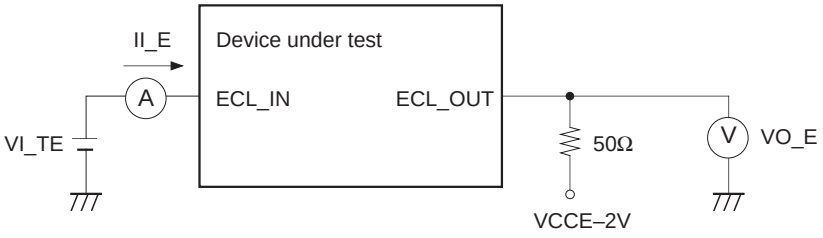


(a) TTL I/O DC characteristics measurement circuit

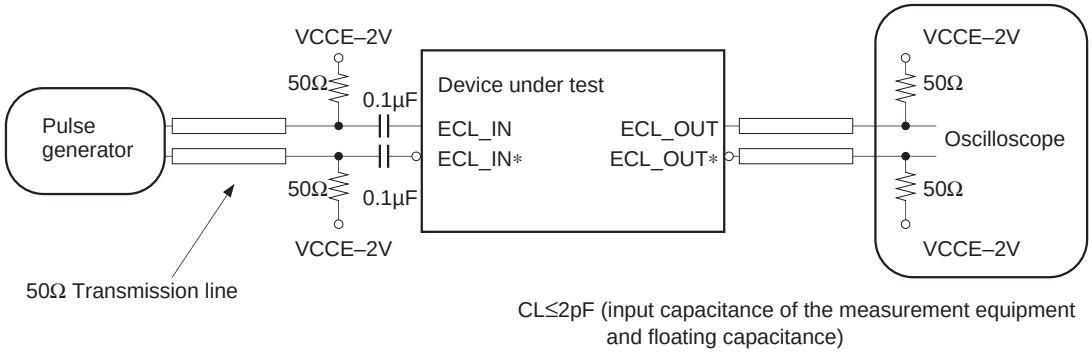


CL=10pF (including the probe capacitance)

(b) TTL I/O AC characteristics measurement circuit

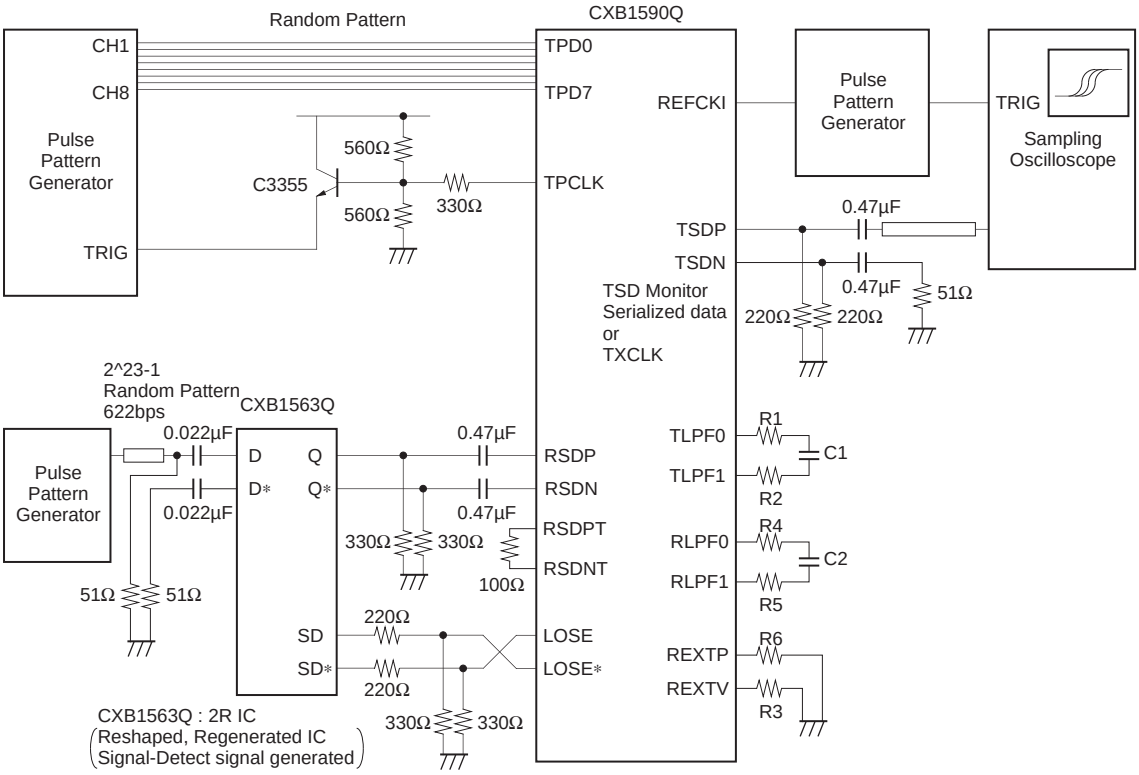


(c) ECL I/O DC characteristics measurement circuit

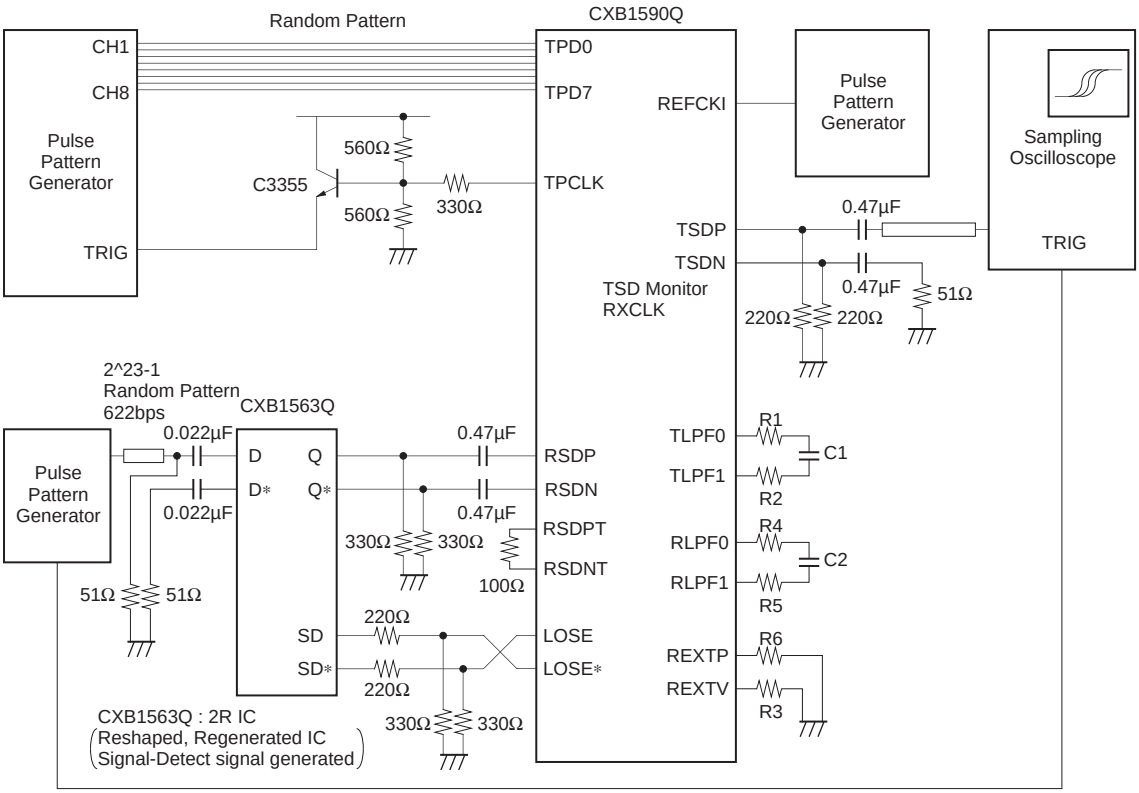


CL≤2pF (input capacitance of the measurement equipment and floating capacitance)

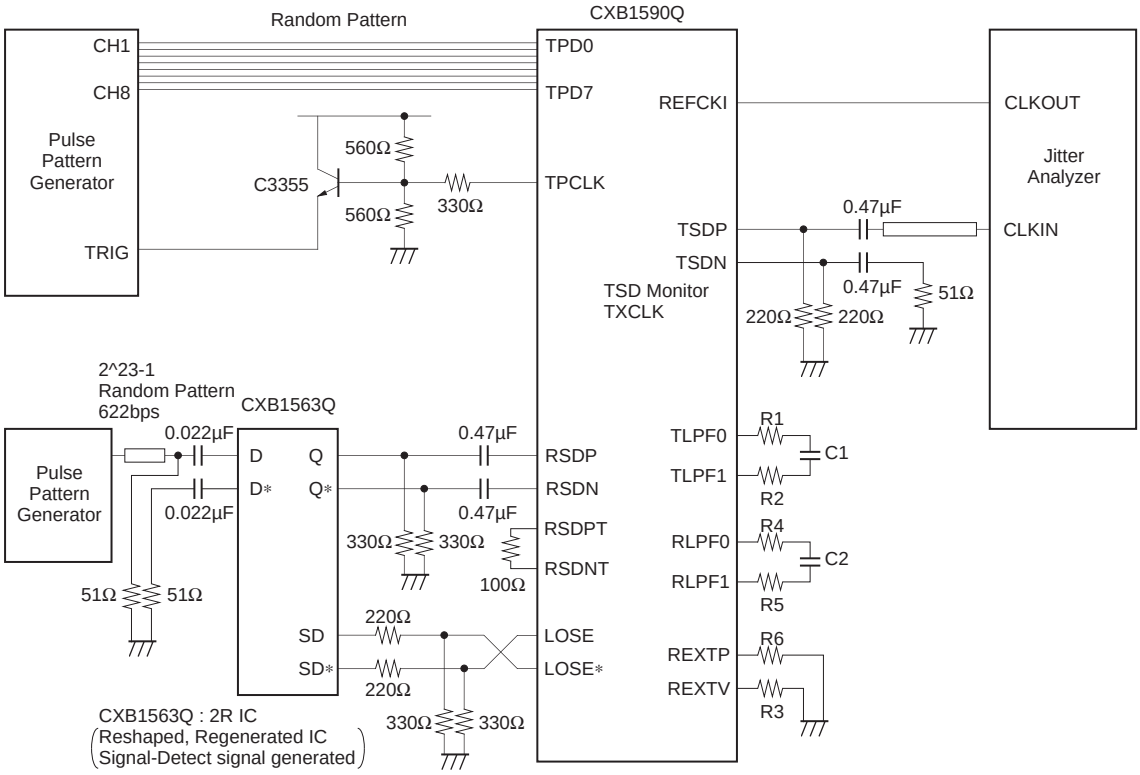
(d) ECL I/O AC characteristics measurement circuit



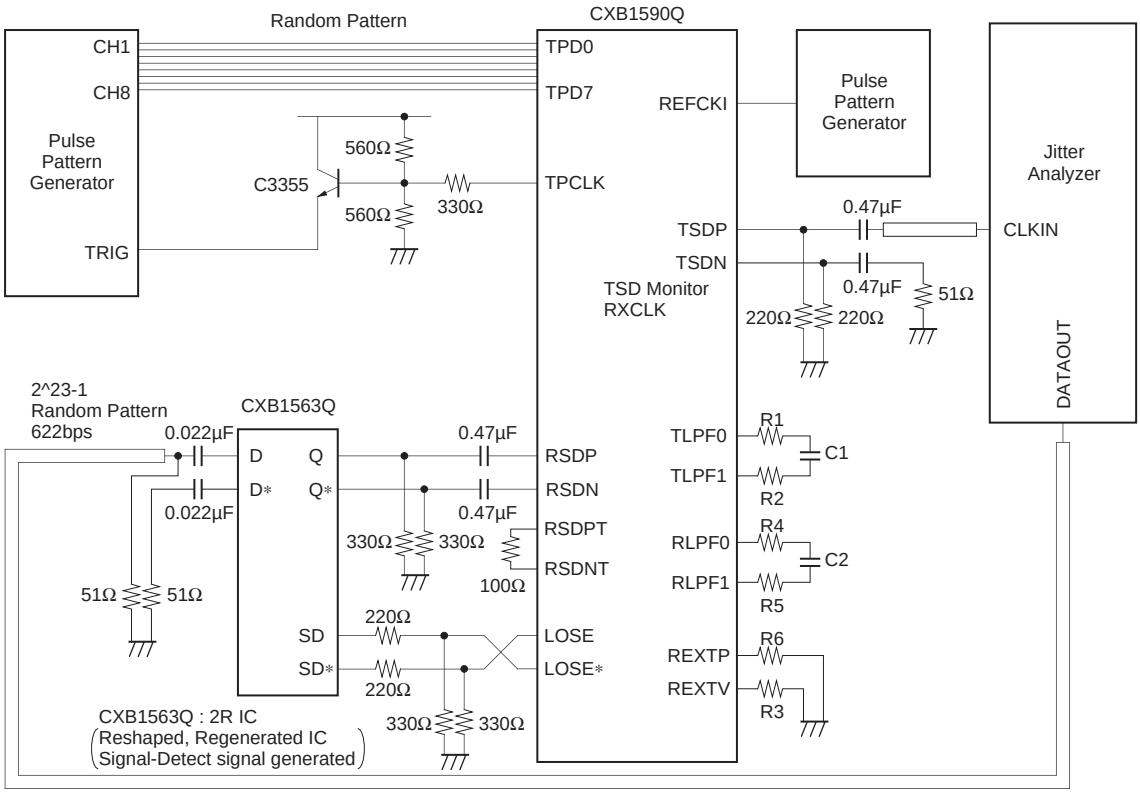
(e) TX random jitter measurement circuit



(f) RX random jitter measurement circuit



(g) TX jitter transfer measurement circuit

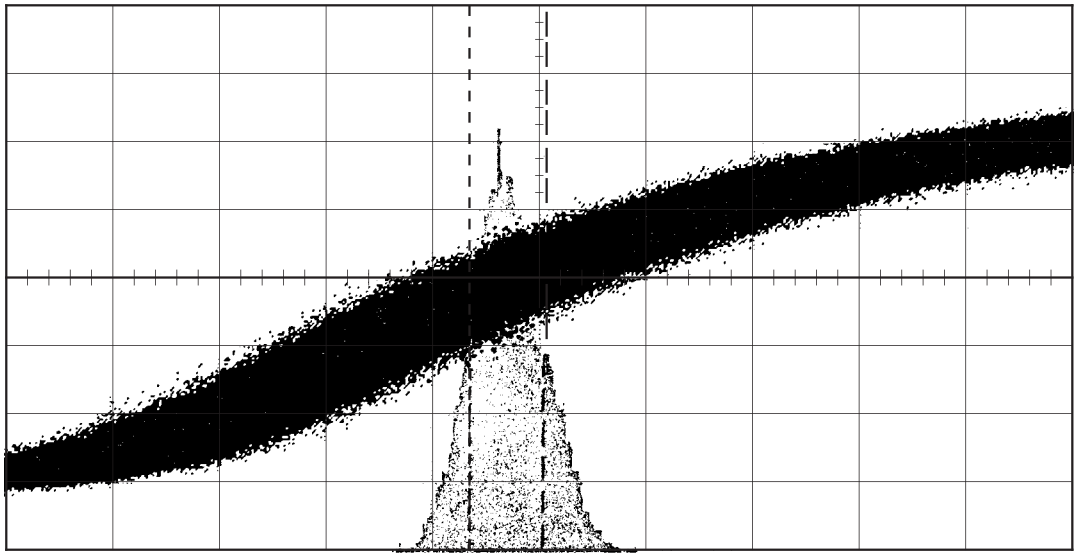


(h) RX jitter transfer measurement circuit

Fig. 10 Electrical Characteristics Measurement Circuit

Example of Representative Characteristics

Example of TX-clock (622MHz) Rj measurement



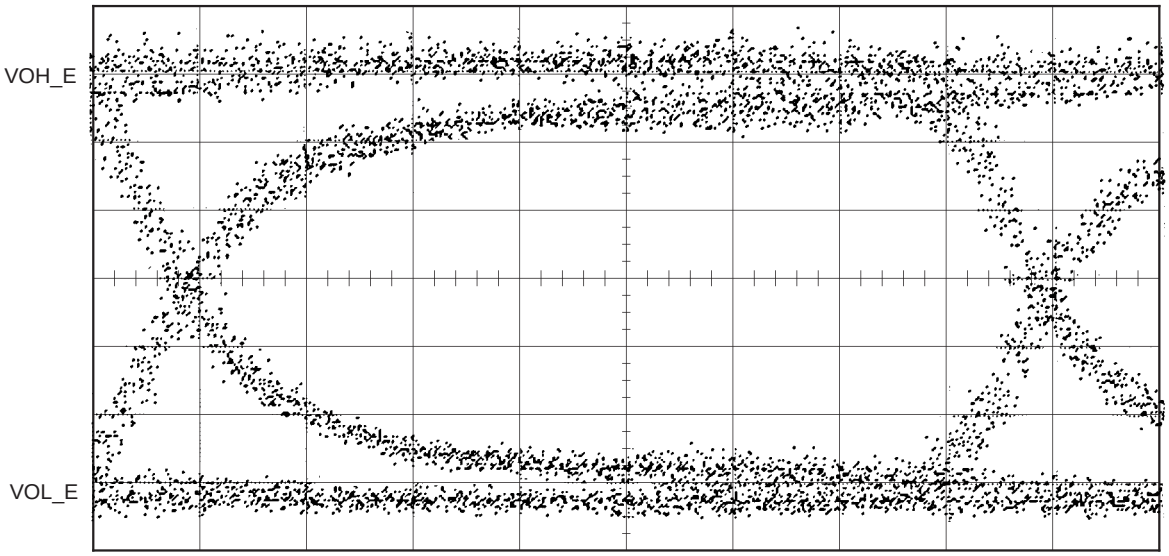
R1=R2=1.0kΩ
R3=1.5kΩ
C1=22nF

REFCKI input 51.84MHz

Rj=17.4psec

x : 50psec/div
y : 100mV/div

Serial Transmit Data Output Eye Pattern (622MHz Operation)

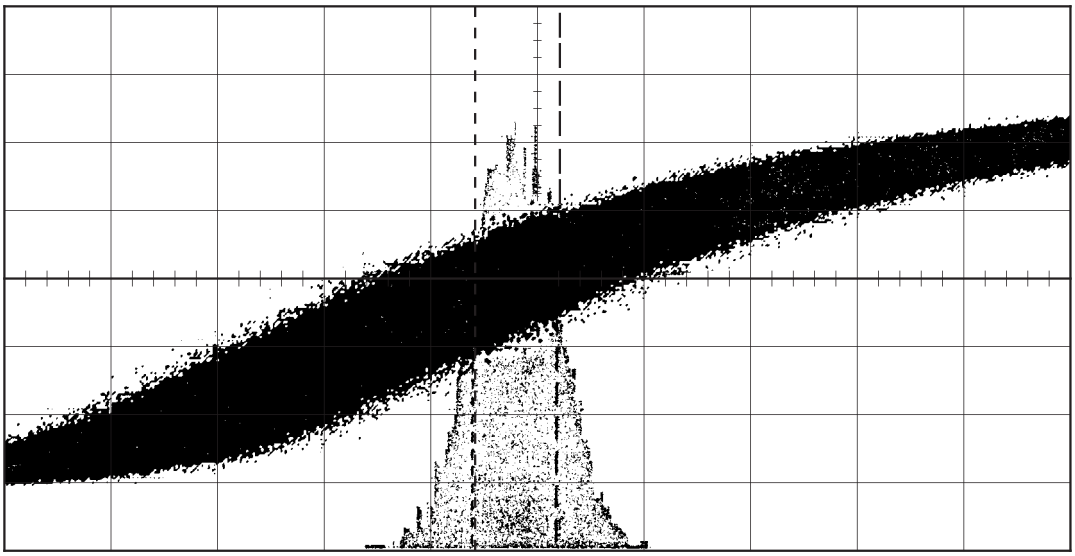


R1=R2=1.0kΩ
R3=1.5kΩ
C1=22nF

REFCKI input 51.84MHz

x : 200psec/div
y : 100mV/div

Example of RX-clock (622MHz) Rj measurement

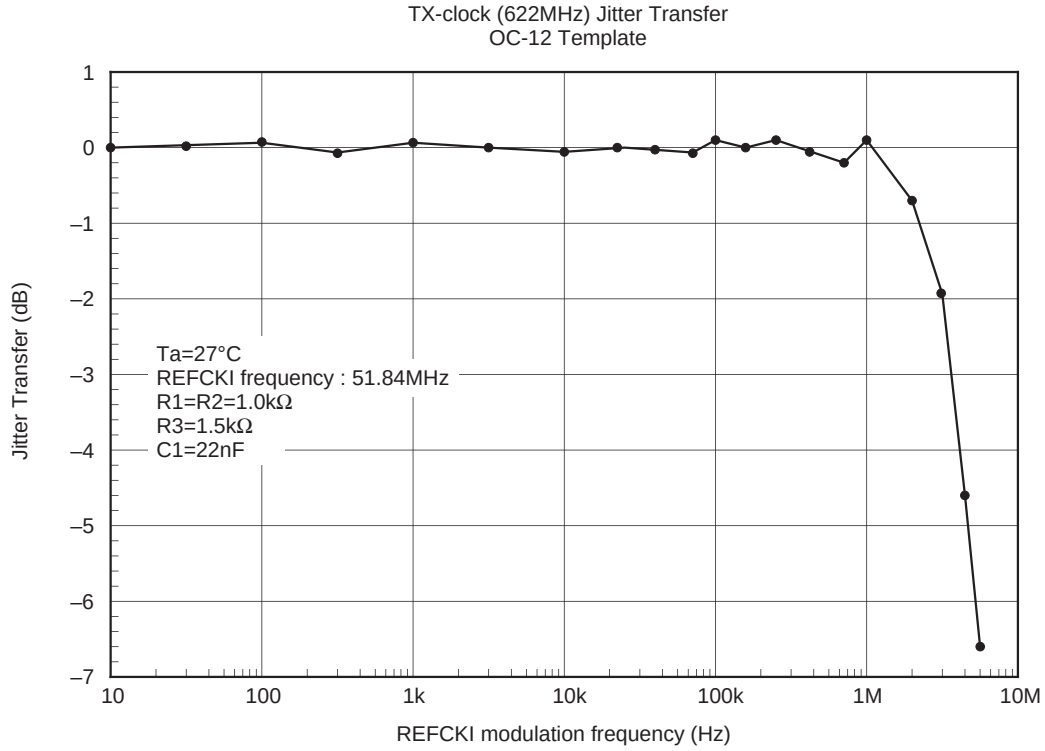


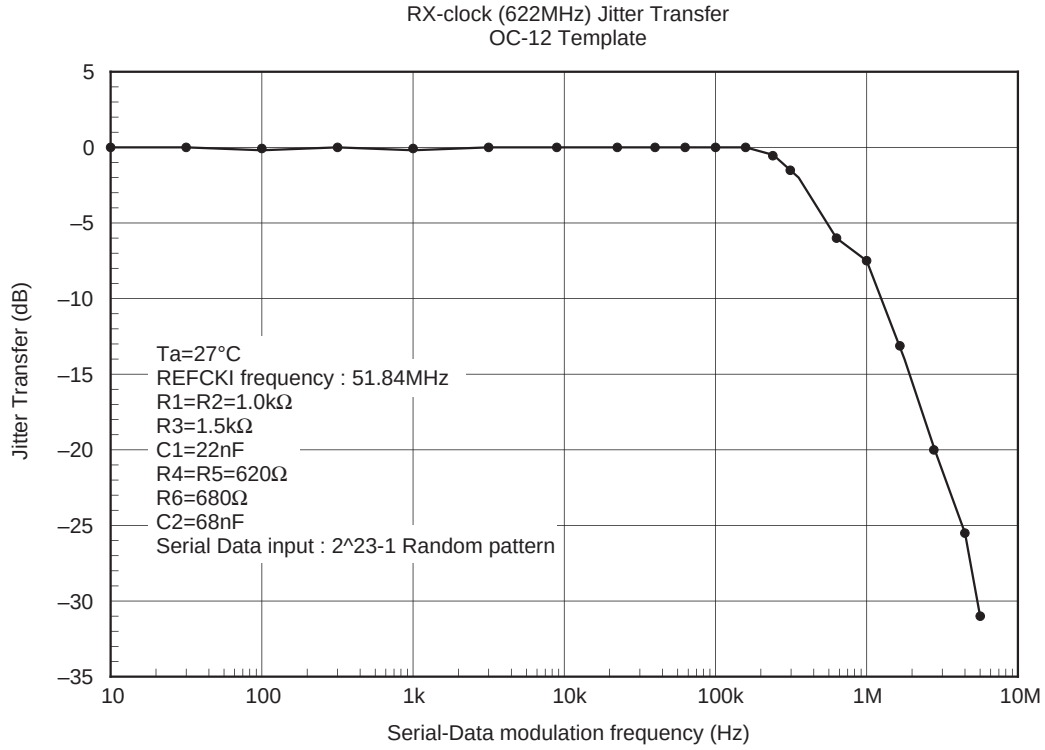
R1=R2=1.0kΩ
R3=1.5kΩ
C1=22nF
R4=R5=1.0kΩ
R6=680Ω
C2=68nF

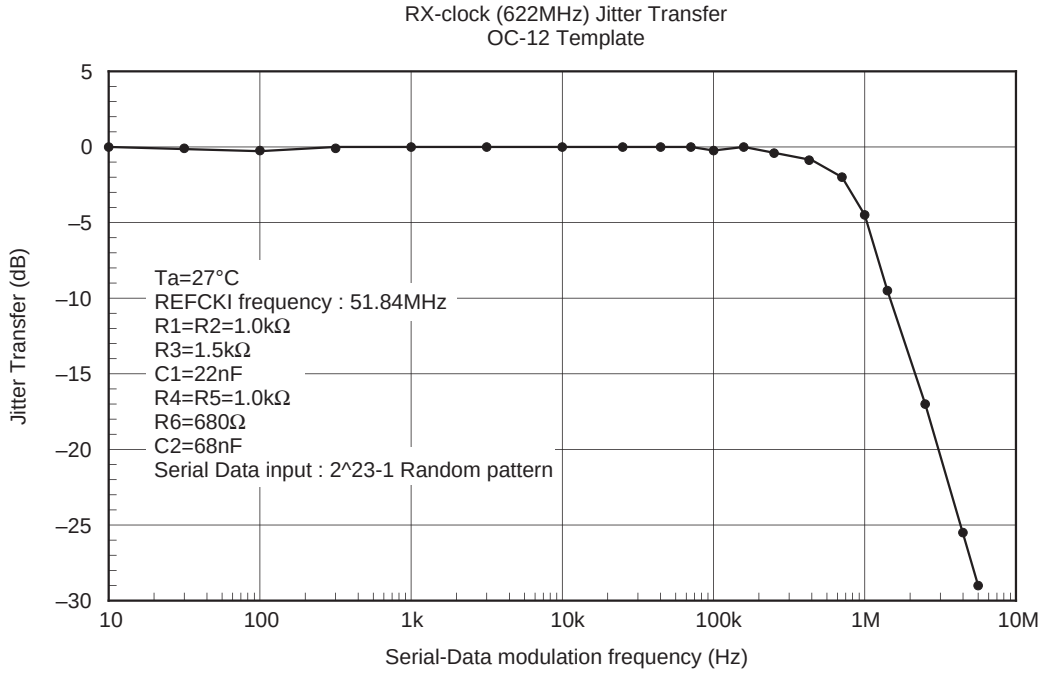
REFCKI input 51.84MHz
Serial Data input 2^23-1 Random pattern

Rj=19.5psec

x : 50psec/div
y : 100mV/div

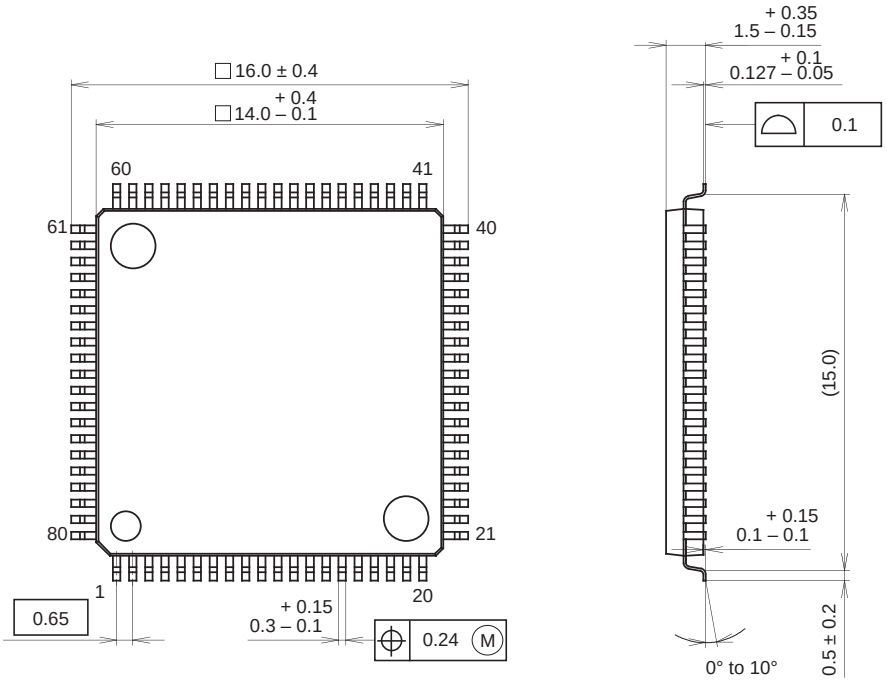

TX-clock (622MHz) Jitter Transfer
OC-12 Template
Jitter Transfer (dB)
1
0
–1
–2
–3
–4
–5
–6
–7
Ta=27°C
REFCKI frequency : 51.84MHz
R1=R2=1.0kΩ
R3=1.5kΩ
C1=22nF
10
100
1k
10k
100k
1M
10M
REFCKI modulation frequency (Hz)


RX-clock (622MHz) Jitter Transfer
OC-12 Template
Jitter Transfer (dB)
5
0
–5
–10
–15
–20
–25
–30
–35
Ta=27°C
REFCKI frequency : 51.84MHz
R1=R2=1.0kΩ
R3=1.5kΩ
C1=22nF
R4=R5=620Ω
R6=680Ω
C2=68nF
Serial Data input : 2^23-1 Random pattern
10
100
1k
10k
100k
1M
10M
Serial-Data modulation frequency (Hz)


RX-clock (622MHz) Jitter Transfer
OC-12 Template
Jitter Transfer (dB)
5
0
–5
–10
–15
–20
–25
–30
10
100
1k
10k
100k
1M
10M
Serial-Data modulation frequency (Hz)
Ta=27°C
REFCKI frequency : 51.84MHz
R1=R2=1.0kΩ
R3=1.5kΩ
C1=22nF
R4=R5=1.0kΩ
R6=680Ω
C2=68nF
Serial Data input : 2^23-1 Random pattern

Package Outline Unit : mm

80PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-80P-L03
EIAJ CODE	QFP080-P-1414
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.6g